Design Document

**Abstract**

A SR Latch, known as set-rest latch, is a bistable device. It can be setup using two NOR or NAND gates in such a way that the output of one feeds back to the input of another and vice versa. The Q and not-Q outputs are supposed to be in opposite states. When they are in the same state, the inputs of the S-R latch are considered to be in an invalid or illegal state. The goal of this project is to design a program that can simulate the behavior of a S-R latch. The inputs would be taken in from a text file and then the program should be setup with either NOR or NAND gates wired to have inputs from the outputs. The program should then determine if the outputs derived from the inputs are valid. If that is the case, the program will state that the inputs are valid for whatever gate is being analyzed. The program should then output all of this to a text file.

**Methodology**

Methods called: nandIdentityS, nandIdentityR, norIdentityS, and norIdentityR will be used to process input data through NOR or NAND gates

ReadTruthTableData() will be used to convert data to true or false (this is not necessary, but is an extension of previous week assignment)

The input data is then run through for loops that will rely on the above Identity methods to process the data

Final output will be text file that shows the generated Q and not-Q outputs based on the Identity methods and shows true if the generated outputs match actual output. The output file will also show if the input and outputs are valid for a S-R latch.